CPLD-Controlled PICNIC Camera at IOTA

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ABSTRACT

We describe a new near-infrared camera based on the PICNIC array for the Infrared-Optical Telescope Array (IOTA). The camera control is based on a complex programmable logic device (CPLD). This architecture allows fast and stable clocking of the PICNIC array, resulting in faster and lower-noise readout. The CPLD architecture also allows on-the-fly reconfiguration of the readout circuit. We demonstrate this capability with the implementation of circuits dedicated to two different functions: imaging used for alignment purposes, and fast sequential readout of a few pixels used for interference fringe detection.

In fringe detection mode, the measured rms readout noise for a single read of the detector is $\sigma_{\rm single-read} = 8.7 \pm 0.6$ electron. In data-acquisition mode, the signal is the difference of two successive reads, so the noise on this signal is larger by $\sqrt{2}$, giving $\sigma_{\rm read} = 12.4 \pm 0.8$ elec.

With M multiple reads of a given pixel, the read noise averages down as $\sigma_{\rm M} = \sigma_{\rm read}/\sqrt{\rm M}$, for at least the range $1 \leq {\rm M} \leq 16$, showing that fast, multiple reads significantly improve performance in the PICNIC detector.

Subject headings: Instrumentation: interferometry, infrared: detector

1. INTRODUCTION

The IOTA – a collaborative project between the Smithsonian Astrophysical Observatory, Harvard University and the University of Massachusetts at Amherst – is an optical long baseline interferometer located on Mount Hopkins, AZ. The array consists of three 45 cm diameter telescopes able to be relocated along the arms of an L shaped track. The arms of the L track are 15 m and 35 m in length, with south-east and north-east

orientations respectively. The minimum and maximum baselines have length of 5 m and 38 m.

IOTA has operated routinely since 1995 with the first two telescopes that were first installed. Installation of the third telescope started in the summer of 1998 and culminated in February 2002, when first simultaneous three telescope measurements were obtained. For a full description of IOTA and its subsystems see Traub et al. (2000, 2002).

Driven by the requirements of the third-telescope upgrade, the control and data acquisition systems have undergone major changes. The distributed computing network, once composed of separate computers running different operating systems, has now been replaced by a system based on the VME bus (a real-time, control oriented computer architecture) and the real time operating system VxWorks. These changes have allowed us to cope with the increased real time control and data processing needs introduced by having two new baselines and an additional telescope.

The need for simultaneous combination of three telescope beams also imposes the following new constraints on our fringe detection camera. (1) More pixels need to be sampled, as any beam combiner design will have more outputs than for the two-telescope case. (2) Each beam combiner output contains less light from each telescope, due to the required additional beam splitting. (3) Measurement of the new closure-phase observable requires substantial overlap of interferograms, which have to be measured in the same coherence time. Therefore it is critical for the detection to be made in as short a time as possible compared to atmospheric piston time scales. Thus, building on the success of our previous NICMOS3-based infrared instrumentation (Millan-Gabet 1999; Millan-Gabet et al. 1999) we have upgraded our science camera. The new camera, described in this paper, is based on the improved PICNIC array (developed by Rockwell Scientific). Mechanically, the new dewar is an improved version of that of the previous camera, but now hosts two

motorized filter wheels which will allow us to conduct near-IR narrow-band observations.

The most important difference in the new camera over the previous NICMOS3 system is the use of CPLDs (Pedretti et al. 2002) as control electronics, to substitute for the previously-used PC based programmed I/O approach.

A block diagram of the overall control system is shown in Fig. 1. In this section the CPLDs are located in the blocks labeled "Technobox". The CPLDs allow faster and jitter-free clocking of the detector, which benefits our measurements in three distinct ways. (1) Minimum clocking noise is expected due to the fact that our jitter-free clocking results in very constant effective integration times from sample to sample. (2) Lower effective noise results from being able to average a larger number of reads within the same total integration time per sample. (3) With lower noise, faster readout allows faster detection of interferograms with no loss in signal to noise ratio (SNR), ultimately improving the calibration of visibility amplitudes and closure phases as indicated above. Moreover, this method unloads the CPU from clocking tasks, freeing-up time which can be better spent in our also-new active fringe tracking task, described elsewhere (Pedretti et al. 2003).

The fast readout of a few pixels is very specific to interferometry. IOTA is and will be a testbed for new schemes of beam combination. This will likely require reconfiguration of the pixels being read, and the current camera readout scheme is well-suited to provide this flexibility.

2. CAMERA ELECTRONICS

2.1. The PICNIC Detector Array

The PICNIC focal plane array (Kozlowski et al. 2000; Cabelli et al. 2000) is composed of four 128×128 pixel quadrants of a HgCdTe detector which are addressed simultaneously

and independently. The active area of each pixel is $(40\ \mu m)^2$. The PICNIC detector is an evolved version of the NICMOS3. Both detectors are hybrid devices: a small band-gap material (HgCdTe) on an insulator substrate (sapphire) interconnects through indium bumps to a silicon substrate, where circuitry for addressing the pixel and analog electronics are built. The quantum efficiency of the individual detectors is better than 50% for wavelengths in the range 0.8-2.5 μm. Our PICNIC camera is equipped with standard near-infrared broadband filters: J (1.11–1.39 μm), H (1.50–1.80 μm) and K$'$ (2.00–2.32 μm), as well as a variety of narrow-band filters within the those bands.

The main differences between the NICMOS3 and PICNIC arrays are in the silicon substrate (sometimes called the multiplexer). (a) In an attempt to reduce the effects of noise caused by resetting pixels in the array (reset anomaly), PICNIC has a line by line reset instead of a pixel by pixel reset. (b) The LINE and PIXEL clocks (cf. Section 2.5) used to address the pixels of the detector are both double-edged for the PICNIC detector whereas they are single edged in the NICMOS3. (c) The output source follower, used to read the pixels in the PICNIC array, can be turned off when not in use in order to decrease the effects of the output source follower glow. (d) In the NICMOS3 array it is possible to address each quadrant separately, but for PICNIC a single set of bias, clocking and output lines are available to the user and the four quadrants must be operated in parallel.

2.2. Analog Electronics

The analog electronics of our new PICNIC camera are identical to the electronics used in the IOTA NICMOS3 camera (Millan-Gabet 1999; Millan-Gabet et al. 1999), with the exception of the printed circuit board (PCB) on which the detector itself is mounted (since the PICNIC and NICMOS3 carriers are not pin-to-pin compatible).

Our NICMOS3 analog electronics design was very successful in avoiding noise induced by the digital circuitry. All digital signals and ground arriving from the outside world are de-coupled from the camera analog electronics by using opto-isolators. The PCBs are carefully designed to separate the local digital ground of the opto-isolators from the analog ground. Separate digital and analog ground planes were laid out around digital and analog components in order to shield out interference from the switching of the opto-isolators and other digital circuits. Both grounds are connected to the metal chassis at a single point to avoid ground loops. All the interconnection cables to and from the dewar are shielded to avoid electromagnetic interference.

Nevertheless, in the new camera and in the new laboratory environment that resulted from the substantial upgrades made to most of our sub-systems, we experienced some interference problems, attributed mostly to the delay lines' power electronics and to a lesser extent to VME real-time control system rack. After these problems were solved we were left with some residual, high frequency noise, increasing the camera noise to about 20 electrons. This, we discovered, was due to a bad ground network which was injecting noise into the camera. A solution which we found viable was to protect the sensitive electronics with a choke wound around a ferrite bead, connected in series to the ground connection of the PICNIC camera. This solution, although not ideal, eliminated this source of noise.

2.3. CPLD Technology

A digital circuit is built by connecting several devices which perform logic functions. Such devices usually provide standard functions of different complexities, starting from simple logic functions such as Small Scale Integration (SSI) and Medium Scale Integration (MSI) Transistor-Transistor Logic (TTL) devices and ending in high performance full custom designs such as microprocessors and random access memories. Full custom design

requires years of development and test and is used when high volume production is required.

CPLDs and FPGAs (Field Programmable Gate Arrays) permit the implementation of complex digital circuits on a single chip. CPLDs tend to have faster and more predictable timing properties, while FPGAs offer the highest gate density (Hamblen & Furnan 2000). The number of gates in the chip is on the order of hundreds of thousands and this number is increasing rapidly while the technology improves. In the Altera Flex-10K70, used in the PICNIC IR-camera at IOTA, gates can be interconnected to form complex networks using electronic switches; the switch interconnections are stored on a static RAM, so the interconnection among elements can be changed in just milliseconds. This means that a single component can host several circuits performing very different functions at different times.

We developed our circuits on a commercially available PCI-PMC[7] card which contained an Altera 10K70 CPLD. This card plugs directly into the PMC connectors of our CPUs. The advantage of this configuration is being able to load a new circuit in the CPLD from the CPU memory or from the disk during operation. The disadvantage of this configuration, as we discovered, is in forcing outputs to be be assigned to specific components and I/O pins. The compiler prefers that the pins are freely assigned the first time it builds the circuit, in order to optimize the routing of signals. Fixed output pins likely add delays to the circuit which makes it failure prone at higher speed. Another disadvantage of using a PMC interface is the impossibility of using an oscilloscope probe on the component; also the real time debug tools which permit the physical testing of the timing on the component can only be used with the ALTERA programming interface and software, complicating the

[7]A card based on an interface electrically identical to a standard PCI bus used in personal computers but implemented with a different type of connectors (following the PMC standard definition). This card connects the CPLD to the CPU card.

debugging process.

2.4. The VxWorks Real-Time System

The new control system for the IOTA interferometer is centralized in a VME type computer. VME is an industrial standard defining the mechanical and electrical characteristics of a computer bus, oriented to instrumentation control. CPUs based on different processors can be plugged into the bus.

Real-time means that the different tasks are executed at very precise intervals in time, synchronized by a "real time clock" which defines the pace of the system. This is crucial for instrument control (in our case controlling visible and IR cameras, telescopes, delay lines, fringe trackers and data storage).

The VxWorks system is UNIX hosted, meaning that all the development can be done on a UNIX computer, using standard cross-compilers (GNU) editors, etc. UNIX is not per-se a real time system. The UNIX computer host (in our case a SUN Blade-1000) is connected to the VME rack through a fast optical link and communicates with three CPU targets. The SUN host loads the compiled programs on the targets and these programs (tasks) are executed using the VxWorks operating system, which is basic and streamlined, but allows us to use standard UNIX sockets to communicate with UNIX based workstations, file-servers, etc. with a standard Ethernet connection.

2.5. Clocking the Detector

The detector matrix is addressed through two shift registers The vertical shift register for lines is controlled by the [LINE , FSYNC] clocks. The horizontal shift register for pixels

is controlled by the [PIXEL, LSYNC] clocks. FSYNC and LSYNC act as reset for the shift registers (active low): when they are asserted the respective registers are loaded with all ones. The LINE and PIXEL clocks are double edge clocks. The first rising (or falling) edge connects the line or pixel circuitry to the output of the detector; the second falling (or rising) edge will put a zero in the first bit of the corresponding shift register. Each of the following clock edges will shift the zero by one position (bit) in the register; the zero bit will enable an analog switch to read the corresponding line and pixel of the detector.

Before reading the detector the pixels must be connected to the bias potential, in order to charge the junction capacitance (reset). The PICNIC multiplexer resets a whole line at a time (an important improvement in speed and performance compared to the NICMOS3 detector, where the pixels were reset one at a time) by asserting the RESET clock (active high) together with the LINE clock.

After reset, the reset bias voltage appears across the detector pixels. Subsequently, photo-electrons are generated and the voltage decreases linearly with incident flux, until the pixel voltages are zero, at which point the array is *saturated* and needs to be reset again in order to be responsive. A variety of clocking methods are possible for measuring the incident flux integrated during a given time. Two such methods will be described below, but in general always involve resetting the array or pixels of interest and then differencing the (amplified and digitized) output voltages corresponding to two consecutive reads separated by the integration time.

2.6. Implementation of the Quadrant Readout Mode

Although the camera's principal use is reading out a small number of pixels illuminated by the beam combiner, it is necessary to read a whole quadrant for optical alignment

purposes. Moreover, in this mode the camera could be used as an IR wavefront tip-tilt sensor, to track sources which are too faint at visible wavelengths to be observed using our current CCD-based system. A block diagram of the CPLD circuit in quadrant mode is shown in Fig. 2.

2.6.1. Correlated Double Sampling

In correlated double sampling (CDS) mode, adopted for quadrant readout, the detector is reset, sampled (reset frame), allowed to integrate and re-sampled (image frame). The difference between the reset and image frames is then recorded. This is the basic operational mode of the NICMOS3 and PICNIC detectors, both of which are integrating detectors, with non-destructive readout. CDS is implemented entirely in the CPLD electronics. The CPU receives a buffer containing the final, ready to use, data. Unless otherwise stated, in this paper we will use the term "read" to mean a CDS read cycle.

2.6.2. Circuit Implementation

The quadrant image read is stored in the static RAM (SRAM) on the Technobox PCI-PMC card, which is shared between the CPU and the CPLD through the PCI bus. The readout starts when the start bit in the control register of the CPLD is asserted by the CPU. The interrupt line (INTA) is asserted when the readout process has finished and a frame is present in the SRAM.

Between these events, many operations are handled in parallel by state machines which have been built into the CPLD. These state machines are as follows.

1. SRAM state machine, which handles communications with the PCI bridge for bus

arbitration. It polls the start bit of the control register and sets a semaphore which starts the LINE state machine. When a reset frame and an image frame have been acquired and subtracted, it releases the PCI bus and asserts INTA.

2. LINE state machine, which controls the FSYNC and LINE clock generation for the PICNIC array. Once a line has been selected it sets a semaphore to start the PIXEL clock generation; lines are counted by the line counter. It will also assert the RESET line, together with LSYNC if the toggle flip-flop, which keeps the state of the frame (reset-frame or data-frame), is set on reset-frame.

3. PIXEL state machine, which controls the LSYNC and PIXEL clock generation for the PICNIC array. It controls the sequence of clocks and sets a semaphore when the analog to digital converter (ADC) can sample the selected pixel; pixels are counted by the pixel counter.

4. ADC state machine, which controls the ADC. If the toggle flip-flop is in reset frame state, then the ADC state machine sends a start of conversion pulse to the ADC, waits for the end of conversion signal from the ADC, and writes a word of data in the static RAM. If the toggle flip-flop is in data-frame state, then the ADC state machine stores the difference between the data word at the current SRAM address and the data word obtained from the ADC. The SRAM address is obtained by combining the line counter and pixel counter.

5. READ-SRAM state machine, which reads one word of the reset frame previously written to SRAM, during the ADC conversion. This operation is carried out in parallel with the ADC data conversion. The data previously stored in memory, and addressed by the ADC state machine, is recovered and stored in a temporary register. This value will be used to calculate the difference between the reset value and the current value obtained from the ADC converter.

The data acquisition (DAQ) scheduler task, running on the CPU when in quadrant mode, loads the circuit into the CPLD and initializes the readout parameters. The start bit is then asserted in the CPLD control register, the state machines are started and the controller runs in a loop until a whole quadrant is acquired.

2.6.3. Readout Parameters

A number of readout parameters can be changed by the application running on the CPU by accessing the registers on Altera. The registers are as follows.

1. T_{base} is the PICNIC base clock period. The 33 MHz PCI clock is divided by a programmable counter built into the CPLD, in order to generate the base clock rate used to clock the PICNIC array; the counter can be programmed by the CPU through the PCI bridge. A typical value is 1 μs.

2. T_{del} is the delay between the PICNIC clock and the sample assertion to the ADC. This delay is necessary to avoid sampling the addressed PICNIC pixel before it has settled. The delay is generated by a programmable counter and is accessible to the CPU through the PCI bridge. A typical value is 4 μs.

3. T_{int} is the integration time. This is also a presettable counter which determines the time between the reset frame and the image frame. A typical value is a few ms.

4. (N_x, N_y) is the sub-quadrant corner position in units of pixels (cf. Sec. 2.7.6). With these variables it is possible to define a small area of the detector. This flexibility will be crucial when implementing an IR wavefront tip-tilt sensor.

2.7. Implementation of Interferogram Detection Mode

This mode reads a number of pixels located at arbitrary coordinates on the PICNIC array, for detection of interference fringes. In practice, for better clocking efficiency and noise performance the pixels should be closely spaced and, preferably, on the same line. A block diagram of the CPLD circuit in interferogram detection mode (also sometimes called scan mode) is shown in Fig. 3.

2.7.1. Fringe Detection and Sampling

A brief description of how interferograms are produced at the IOTA is required before we describe our sampling method.

Starlight collected by each telescope enters a vacuum enclosure (in order to avoid chromatic dispersion) as afocal beams of 45 mm diameter. The change of optical path introduced by the sidereal motion of the star is compensated by sending the beams from two of the telescopes to two separate delay lines. After the delay system, the telescope beams exit the vacuum and enter the beam combination laboratory, located at the center of the array. For near-IR science operation, three dichroics transmit visible light towards the wavefront tip-tilt sensor, and reflect near-IR light into the beam combination table.

Three-way beam combination at the IOTA was first achieved using the H-band integrated optics component, IONIC-3T, developed by the IONIC collaboration in Grenoble[8] (Berger et al. 2002). In the following, we refer to this setup, and show sample data obtained with it.

[8]The IONIC project is a collaboration between LAOG, LETI and IMEP, Grenoble, France.

Near-IR light is directed towards three flat steering mirrors and then three off-axis parabolas, which focus the three beams into three fibers feeding the IONIC-3T component. In this component, each input is first divided into two parts. Interference then takes place pair-wise inside the component, resulting in six output beams comprising three complementary pairs. Each output interferes the light from a pair of telescopes. The six output beams are then focused onto six separate PICNIC pixels. The interference fringes are recorded while two of the dichroics are piezo-driven to scan a path of 100 μm and 50 μm in order to modulate the optical path difference (OPD). A scan typically contains 256 data points.

2.7.2. Differential Sampling

With this method, adopted in fringe detection mode, the array is reset only once, at the start of each scan, then the pixels of interest are sampled continuously as they discharge. Each data point in the scan is the difference between consecutive samples, and the integration time per data point is set by the time needed to sample each target pixel, possibly multiple times, as described below. Avoiding the array reset for every data point reduces the noise, and increases the readout speed, but at the expense of dynamic range.

2.7.3. Circuit Implementation

The digitized pixel voltages are stored in SRAM. INTA is asserted at the end of every group of pixels which are read out. INTA is used to delimit the end of a data frame but it is also used to step the piezo OPD scanner which is synchronous with data acquisition. This simple cycle is executed once per data point (e.g., 256 times per scan) and stored in memory as a time sequence. When one scan is finished a flag is asserted in the control

register and the CPU transfers the stored vector to a buffer.

Following the same methods implemented in the previous NICMOS3 camera, each time a pixel is accessed it can be sampled several times and the values added and stored in a register; we call this *reads*. It is also possible to read the whole group of pixels and sum the values separately; we call this *loops*. By averaging the $N = loops \times reads$ samples, the readout noise is ideally reduced by the factor $\sqrt{N}$. Using many reads achieves a better SNR but increases the latency between sampling different pixels; using many loops degrades slightly the SNR since it involves clocking the detector, which adds noise, but the time delay among different pixels is reduced. In practice, we choose combinations of reads and loops which are compromises between those two effects.

The hardware implementation of this function is as follows. Data for each pixel must be stored in separate registers and added there, then data is transferred to SRAM and INTA is sent to the CPU through the PCI-bridge. The interrupt must be cleared by the CPU at the end of this process. To limit access to the SRAM and avoid conflict with the CPU, the data is double-buffered in the internal registers, rather than using the SRAM, as is done for the quadrant readout. This unfortunately limits the number of pixels that can be read to nine, since generating internal memory in the CPLD is intrinsically inefficient. This limitation will become important when spectral dispersion is implemented (Ragland et al. 2002) or if polarization splitting is desired, and will be removed in future versions of the CPLD circuit.

The interrupt generated from the CPLD, in addition to informing the CPU that a new data point is available in the SRAM, is also used for stepping a sawtooth modulation of the OPD. This modulation is necessary for acquiring data in fringe mode. The pixel registers, the adders used to integrate the value of the pixels, the counters which count the number of data points transferred, the SRAM address, the internal RAM address and clock generation

are all controlled, as represented by the block diagram shown in Fig. 3, by the five following separate state machines.

1. RES_FRM_PROCESS state machine: resets the whole PICNIC array continuously, clocking lines from 0 to 127 and back to zero. This process is stopped when the start flag is asserted and the main process is idle.

2. MAIN state machine: schedules the N_LOOP_PROCESS state machine and increments the address of the instruction internal RAM which contains the readout sequence transferred from the CPU. It starts when the start bit of the control register is asserted; it clears all registers and starts the loop state machine. It ends when the loop_tc semaphore is asserted.

3. N_LOOP_PROCESS state machine: is scheduled by the main process and decodes the instructions which then generate the detector clocks. These instructions are written in the internal RAM. The internal RAM is loaded by the CPU via the DAQ scheduler program. It schedules the SAMPLE_PROCESS and the SRAM_WR_PROCESS. The LINE, FSYNC, PIXEL and LSYNC clocks are generated by this state machine.

4. SAMPLE_PROCESS: sends start of conversion to the ADC, waits for the end of conversion signal from the ADC, and writes a word of data to the internal register corresponding to the pixel sampled. If the requested number of reads is greater than one, then the state machine reads the ADC several times and the values are accumulated in the corresponding pixel register.

5. SRAM_WR_PROCESS: executes the data transfer to SRAM from the internal registers when the requested loops and reads are completed. When the sequence starts again to sample a new data point it executes in parallel, transfers the data from the pixel registers to SRAM and sends an interrupt when the process is completed.

2.7.4. Micro-coded Instructions

It is highly desirable to have the flexibility of choosing which pixels are sampled in order to use different combiners. For this reason the scanning sequence has to be alterable. This was solved by allowing the state machines to change state according to a program written into a RAM internal to the CPLD. Five instructions can be executed by the state machines as shown in Table 1. These instructions generate a clock sequence; the LINE clock will change level n-times according to the value of the following byte in the program. The same happens with the PIXEL clock, but in this case every pixel is read n-times, according to the value written in the N_{reads} register. Loops are achieved through the jump instruction which permits branching back to a specific instruction in the program. The loop is executed n-times according to the content of register N_{loops}. Arbitrary code for generating a clocking sequence is given in Table 2.

2.7.5. Readout Parameters

In the interferogram readout mode a number of parameters are user-selectable, as follows.

1. T_{base} is the same as in Section 2.6.3 for quadrant mode.

2. T_{del} is the same as in Section 2.6.3 for quadrant mode.

3. N_{loops} is the number of times that the specified pixel group is read. These values are summed in the pixels' registers. A typical value is 4 loops.

4. N_{reads} is the number of times that a specific pixel is read, per loop. It sums the values for that pixel, and puts the resulting sum in the corresponding pixel register. A typical value is 4 reads.

5. Readout sequence. This vector contains the readout instructions used to sample the pixels. The vector contains instructions which assert the lines LSYNC or FSYNC for the detector as well as the LINE and PIXEL lines. Line and pixel instructions have arguments which specify the number of lines or pixels to clock the detector.

6. $N_{samples}$ is the number of samples of each group of pixels acquired and stored into memory. A typical values is 256.

2.7.6. Integration Time

The integration time per sample can be accurately calculated by inspecting the digital circuit in the CPLD. Equation 1 relates the integration time to the digital parameters passed to the circuit.

$$T_{int} = T_{base} \cdot (N_y + 1) + N_{loops} \cdot [T_{base} \cdot (N_x + 1) + T_s + (N_{pix} - 1) \cdot (T_{base} \cdot N_{skip} + T_s)] \quad (1)$$

where

$$T_s = (10\ \mu s + T_{del}) \cdot N_{reads} \quad (2)$$

$$T_{base} = N_{base} \cdot 0.0303\ \mu s \quad (3)$$

$$T_{del} = N_{del} \cdot 0.0303\ \mu s. \quad (4)$$

Here N_x and N_y are the coordinates of the first pixel to be read, measured from the corner of the quadrant where the first pixel is $(N_x, N_y) = (1, 1)$, and N_x corresponds to the PIXEL clock, and N_y corresponds to the LINE clock. N_{skip} contains the spacing between pixels illuminated from the beam combiner. N_{pix} is the total number of pixel sampled (six). T_{base} is the base clock used to generate all the timings for the detector, the ADC, and the CPU through the assertion of an interrupt. It is derived from the system clock period ($0.0303\ \mu s$), multiplied by the digital register value N_{base}.

A delay introduced before sampling the pixel is also produced in the same way, multiplying the system clock by the variable N_{del}. Other parameters are listed in Section 2.7.5. The integration time as a function of the number of loops and reads, calculated from (1) is listed in Table 3. The parameters used were, $N_{del} = 506$ (corresponding to $T_{del} = 15.3\ \mu s$), $N_{base} = 85$ (so $T_{base} = 2.6\ \mu s$), $N_{skip} = 5$, $N_y = 8$, $N_x = 34$. Table 3 is consistent at the 3% level with experimental measured data.

A typical clocking sequence is shown in Fig. 4. The oscilloscope traces show the sample commands to the ADC and the analog quadrant output. The settle and wait time T_{del} is also indicated.

3. Data Acquisition Software

The data acquisition software is composed of two main parts: (1) real time software running on the VME target CPU, written in C/C++, and (2) data visualization and command software, running on the SUN host computer, and written in IDL/C.

3.1. Real-time Software

This software comprises C libraries able to communicate with the CPLD device as well as software responsible for implementing data-acquisition and fringe tracking. The latter is also a new capability at the IOTA, responsible for sensing and servoing the delay locations of the fringe packets, which fluctuate rapidly with the atmospheric differential piston. The algorithm used to sense the fringe phase and the performance of this system will be described in detail in an upcoming publication (Pedretti et al. 2002, 2003)

3.1.1. The C libraries

The CPU is interfaced to the Altera CPLD using a PMC bus, as described earlier. The kernel of this library is given by the manufacturer of the card (Technobox). This is only an example which can be modified by the user according to the CPLD programming. The modules dealing with the PCI bridge and the remote programming of the CPLD do not need any modification.

Two basic functions are associated with the library: (1) writing to the control register to modify the behavior of the CPLD, and (2) reading the static RAM and transferring its contents to a data buffer.

3.1.2. Fringe-tracking and Data Acquisition Software

The functions performed by this module are complex and numerous and they can be broken in these following groups.

1. Switch between quadrant acquisition and scan acquisition mode.

2. Transfer data from the CPLD SRAM to the target CPU RAM any time an interrupt is generated from the CPLD and the END_DATA flag is set in the CPLD control register, in quadrant or scan mode.

3. Generate the scanning ramp sent to the piezo mirrors through the programmable DAC card controlled by the target CPU; every sample of the digitally generated sawtooth-like waveform is passed to the DAC card after an interrupt is received. Offsets generated by the fringe tracker are also added to this waveform.

4. Invoke the fringe tracker routine any time the data has been transferred to memory

and send offsets to the delay line to compensate the slow drift of the optical path with time.

3.2. Data Display and Control Software

The main function of this software suite, written in the Interactive Data Language (IDL), is to provide a graphical interface to the user and send commands to the real-time system, in order to: (1) optimize the optical alignment of the system, (2) display in real time the data being acquired and the performance of the fringe-tracker, and (3) provide an interface for user selection of the parameters of the data acquisition and fringe-tracking systems.

An example of a frame acquired in quadrant mode is shown in Fig. 5, it depicts the six pixels illuminated by the IONIC-3T component outputs. Fig. 6 shows example interferograms obtained in fringe detection mode.

4. DETECTOR PERFORMANCE

4.1. Read Noise and Gain Measurements

The read noise was measured using the standard Poisson-statistics method (e.g., Millan-Gabet et al. (1999)). A light source connected to an adjustable regulated DC power supply was used to provide varying degrees of illumination to the array. For each DC-voltage setting, we recorded scans identically as in science fringe acquisition mode, i.e., 1 loop, 1 read, 6 pixels, and 128 read cycles (129 samples). Two combinations of base clock speed (T_{base}) and pixel sample delay (T_{del}) were used, i.e., (2.5 μs, 15 μs) and (1.0 μs, 4 μs). The corresponding integration times are 310 μs and 130 μs per pixel. The 310 μs

value was selected to be representative of a relatively slow readout; on the other hand, the 130 μs value is the fastest readout speed that we have used, based on recommendations by Rockwell. The measured mean (adu) and variance σ^2 (adu^2) for each pixel are plotted in Fig. 7.

We assume that read noise from the detector and electronics, as well as the photoelectron noise from the incident light beam, each have Poisson statistics. The gain g (elec/adu) is then the inverse of the slope of the variance vs mean curve. The read noise is derived from the variance intercept at zero mean. The results of these 12 experiments are shown in Table 4.

4.1.1. Gain

A number of conclusions on gain follow from Table 4. (1) The gain does not change significantly when the clocking speeds are changed, as might be expected for the reason given just above. (2) The gain values appear to vary slightly from pixel to pixel, with an rms scatter of 4%; this is not too surprising, since the voltage change per electron at the detector pixel is the inverse of the capacitance, and this quantity could easily vary slightly from pixel to pixel. (3) The gain values are nominally independent of pixel position, with a mean value of $g = 2.34 \pm 0.03$ elec/adu, where the uncertainty is the error in the mean.

4.1.2. Read noise

The corresponding conclusions on read noise are as follows. (1) The read noise is slightly higher for the longer integration time samples, i.e., 13.3 ± 1.1 elec for 310 μs integration, compared to 11.4 ± 0.9 elec for 130 μs; more experiments need to be done to see if this effect is real, and what its cause might be. (2) The read noise varies significantly

from pixel to pixel, with an rms scatter of 22%; this suggests that it would be profitable to select an optimal set of pixels in future experiments, although in the present work no attempt was made to select particular pixels. (3) The read noise has a mean value of $\sigma_{\rm read} = 12.4 \pm 0.8$ elec, where the uncertainty is the error in the mean; the $\sigma_{\rm read}$ value refers to the rms variation in the difference of two successive reads, so the single-read rms value may be inferred to be smaller by $\sqrt{2}$, giving $\sigma_{\rm single-read} = 8.8 \pm 0.6$ elec.

4.2. NICMOS3 and PICNIC Comparison

4.2.1. Read noise

It is instructive to compare the performance of our previously-developed NICMOS3 system (Millan-Gabet et al. 1999) with that of the PICNIC system as presented in this paper. When we embarked upon the upgrade from NICMOS3 to PICNIC, we did so in part because the latter was expected to have an unspecified but nevertheless somewhat smaller read noise than the former. We note that the amplifier electronics design is basically the same for both systems, although there are several small differences, and in any case, the readout systems are physically distinct, i.e., we use separate electronics. From the NICMOS3 paper we quote a read noise of 24.6 electrons per difference of two successive reads, in the readout mode normally used for fringe detection, i.e., using loops and reads to access the two output pixels. The corresponding read noise for the present PICNIC system, as discussed above, is 12.4 electrons per difference of two successive reads, in normal fringe-readout mode where loops and reads are used to access (in this case) six pixels. *Thus the PICNIC system has a smaller read noise by a factor of 2.0.* This improvement is likely due to the chip itself as well as improvements in our electronics, but since the chips are clocked differently, we could not use the same electronics for both chips, and therefore we cannot determine what part of the improvement is due to the chip itself and what part is

owed to the electronics.

4.2.2. Clocking speed

PICNIC clocking is faster than NICMOS3 clocking, for several reasons. Faster clocking indirectly helps to reduce noise in a given amount of observing time because more reads per second (see Sec. 4.3) produces lower net noise per second. (1) The pixel clock in PICNIC triggers on both the rising and falling edges of the clock waveform, whereas in NICMOS3 the trigger was only single-edged. The gain is a factor of 2 in clocking along the pixel (x) direction. (2) The PICNIC clock is faster than the NICMOS3 clock, 1 MHz vs 0.3 MHz, giving an additional faster of 3 gain in speed.

4.3. Noise Reduction with Multiple Reads

We also measured the reduction of read noise with multiple sample averaging. We recorded 128-sample data sets with no illumination on the detector under various readout modes, from 1 to 16 reads per sample. Dark current as well as a possible background light leakage would contribute extra counts and associated variance to the data with longer integration times, so to remove this effect we computed the mean value (in electron units) of each scan, and subtracted this value from the variance (also in electron units) for each scan. The remaining amount of variance is then attributable only to the action of reading each pixel, and the square root of this value is the rms read noise. In Fig. 8 we show these rms read-noise values as a function of the number of reads. Data for both the slow (310 μs) and fast (130 μs) readouts are shown, and both give similar results. For each data set, a linear fit with slope of $-1/2$ is shown, which is the slope expected if the rms read noise were to decrease as the inverse square root of the number of reads. Thus the data shows that the

effective read noise can indeed be reduced by making more reads, and that this technique works well up to at least 16 reads. Therefore to improve the quality of a stellar observation, it is always best to make as many reads as possible, consistent with other constraints such as the atmospheric coherence time (for poor seeing conditions) and the saturation time of the detector (for bright stars). This result for our PICNIC detector is in agreement with that previously found for our NICMOS3 detector (Millan-Gabet et al. 1999).

4.4. Magnitude Limit

Although the present paper is devoted to the PICNIC camera and electronics, it is nevertheless worthwhile mentioning briefly how the camera performs at the IOTA interferometer. A complete discussion of the performance of IOTA with IONIC-3T and PICNIC will be presented in a separate publication.

In (Millan-Gabet et al. 1999) we demonstrated that IOTA was able to make useful measurements at H-band on a star with $H = 6.9$, which was effectively the limiting magnitude. The system components at that time were the IOTA 2-telescope interferometer, a classical beam combiner (i.e., no fibers), and our NICMOS3 camera.

Recently we made a comparable-quality measurement of simultaneous interferograms in H-band on a star with $H = 7.0$, which is very similar to our previous magnitude limit. The system components in this case were the IOTA 3-telescope interferometer, the IONIC-3T beam combiner (using single-mode input fibers), and the PICNIC camera described in the present paper.

Several gain and loss factors enter in to a comparison of limiting magnitudes in the two cases, as follows.

Regarding losses, the new system has only one-half the amount of light per detector

pixel compared to the old system, owing to the extra split required in order to combine the light from a given telescope with that of two (instead of one) other telescopes. Another potential loss could occur with the new system because we are focusing the star onto a relatively small single-mode fiber instead of a relatively large detector pixel, a potential factor of about 0.7 reduction in star flux. Yet another loss might occur due to the finite transmittance of the new (IONIC-3T) beam combiner, which in the lab has a measured throughput of about 0.6.

Regarding gains, the new system has a measured noise level which is lower than in the old system by a factor of about 2.0 (cf. Sec. 4.2.1). Also, the new system can be clocked faster (cf. Sec. 4.2.2), so we can make up to about 6 times more reads per unit time, and therefore achieve up to a factor of 2.4 lower noise. In addition, in the new system we replaced the aging coatings on the siderostats and secondary mirrors of the two original telescopes, for an unknown gain, perhaps a factor of 1.5.

On balance, we see that the potential loss factor is roughly 0.2, but the gain factor is roughly 7, for a net gain factor of 1.4, although this value is relatively uncertain. In fact, we did achieve a slightly fainter limiting magnitude with the new system, so in a rough sense we have validated the gain calculations. More importantly, the value of this gain/loss calculation is that it points out areas where we might achieve yet further gains, for even fainter limiting magnitudes.

4.5. Non-standard Behaviors of Camera

There are several areas in which the camera system performs in a non-ideal fashion, as follows.

4.5.1. CPLD spikes

We observed that our data had frequent and strong spikes superposed on it when the room air temperature near the CPLD was greater than about 70 F (21 C). The spikes were quasi-periodic, and their frequency of occurrence increased monotonically with temperature above this critical value. At worst, there was a spike for every few pixels. The temperature of the CPLD itself was well above room temperature, since it was mounted on top of the CPU of a single-board computer, and was in a card cage slot next to another CPU. The solution is simply to keep the room relatively cool.

4.5.2. Settling time after reset

After a frame reset, we found that the voltage on any pixel was not usable for photometry for a time period of about 50 ms. What we saw during this time was a voltage waveform which looked approximately like a capacitor charging curve, with a superposed oscillation of smaller amplitude. After this time, the pixel voltage followed the expected behavior, i.e., a nearly linear ramp, with slope proportional to incident light intensity. The settling time may be due to our electronics, but we have not yet located the root cause.

4.5.3. Pixel interaction

We focused a bright star on a target pixel, and noted that the resulting signal was nearly constant in time, as expected, until the pixel well was depleted; after depletion the signal was essentially zero, again as expected. (In our case the full well was about 145,000 elec.) However when we sampled the adjacent pixel in the same row, we saw an opposite behavior, with a small constant signal prior to saturation of the target, followed by an increased constant signal after saturation. The magnitude of the increase was roughly 15%

of the target signal. We did not explore this behavior thoroughly, but in the cases we did examine, it appeared to be robustly repeatable. The cause is not known.

5. CONCLUSION

We describe a new CPLD-controlled infrared camera for the IOTA interferometer. The CPLD architecture allows on-the-fly reconfiguration of the readout circuit to achieve different functions on the same hardware. Typical read-out modes include full quadrant, sub-array of quadrant, single pixel, a set of pre-selected pixels, etc., and all of these with a wide range of timing options. This architecture allows fast and stable clocking of the PICNIC array, resulting in faster and lower-noise readout. Faster readout has the significant advantage of being able to sample many more times for a given fringe frequency, thereby improving the readout noise, SNR, integrity of the interferograms in the presence of atmospheric piston, and ultimately the calibration of visibility amplitudes and phases.

In fringe detection mode, the measured rms readout noise for a single read of the detector is $\sigma_{\rm single-read} = 8.7 \pm 0.6$ electron. In normal readout mode the difference of two successive reads is larger by $\sqrt{2}$, giving $\sigma_{\rm read} = 12.4 \pm 0.8$ elec. With M multiple reads of a given pixel, the read noise averages down as $\sigma_{\rm M} = \sigma_{\rm read}/\sqrt{\rm M}$, for at least the range $1 \leq {\rm M} \leq 16$, showing that fast, multiple reads significantly improve performance in the PICNIC detector. Coupled to the recently-installed IONIC-3T integrated-optics three-beam combiner at IOTA, we have successfully measured triple interferograms on stars as faint as $H \simeq 7$. With this level of sensitivity, IOTA can extend its two-telescope programs, on evolved stars and young stellar objects, to imaging mode using three telescopes.

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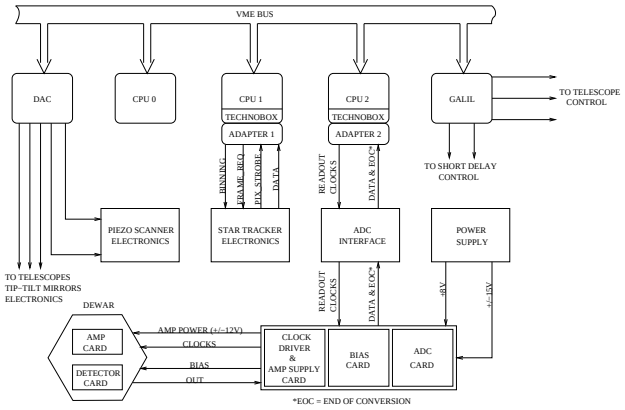

Fig. 1.— Control system block diagram at IOTA. The three CPUs manage different functions of IOTA. CPU-2 is dedicated to data acquisition and fringe-tracking. The CPLD on the Technobox interface performs all the tasks necessary to the PICNIC camera operation.

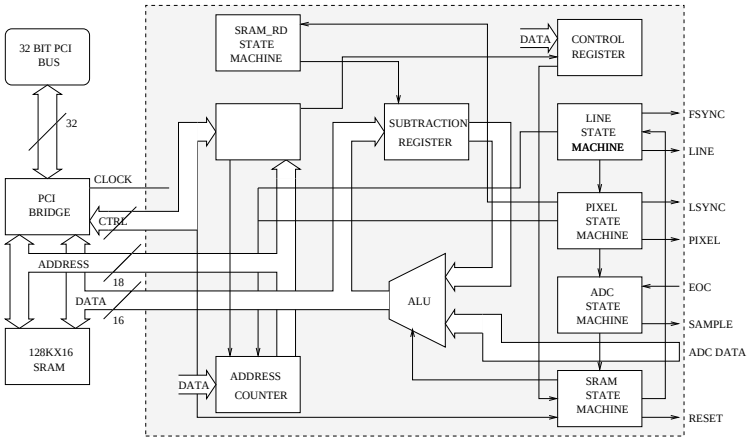

Fig. 2.— The PICNIC quadrant readout circuit. Five state machines are responsible for the operations of the camera. Complex functions are broken into elementary functions of clocking lines, pixels, resetting the detector, commanding the ADC and transferring data into SRAM, each executed by a single state machine.

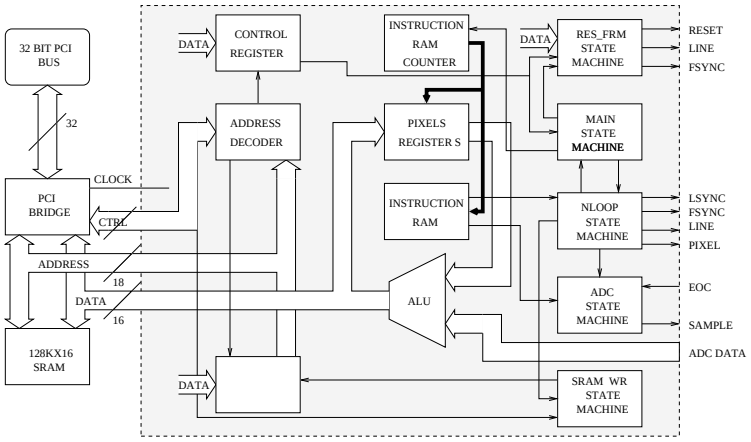

Fig. 3.— Block diagram of the PICNIC camera in interferogram detection (scan) mode. The basic functions are implemented with five state machines. The pixel readout sequence is stored in the instructions RAM, internal to the CPLD. This RAM stores micro-coded instructions specialized to generate clocks sequences for the PICNIC array.

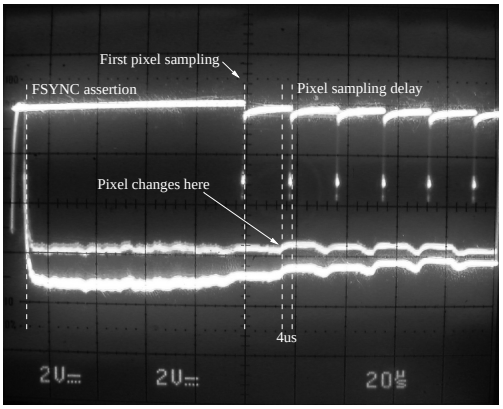

Fig. 4.— The sample command to the ADC and the analog output of the detector are shown in this oscilloscope plot. The time spent between the FSYNC assertion and the first sample signal is the time employed by the PIXEL clock to arrive to the designated pixel. The response of the detector is shown in the lower trace. Also shown is the delay time of 4 μs introduced to allow output settling prior to ADC sampling.

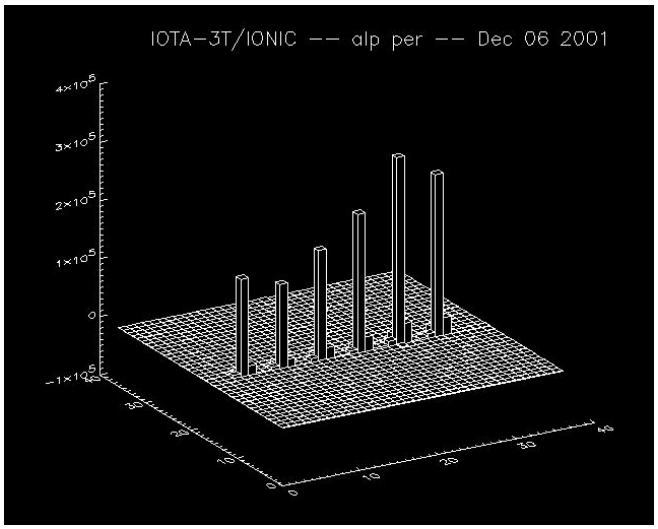

Fig. 5.— An example of frame showing the pixels illuminated by the six outputs of the IONIC-3T beam combiner, imaged in quadrant readout mode.

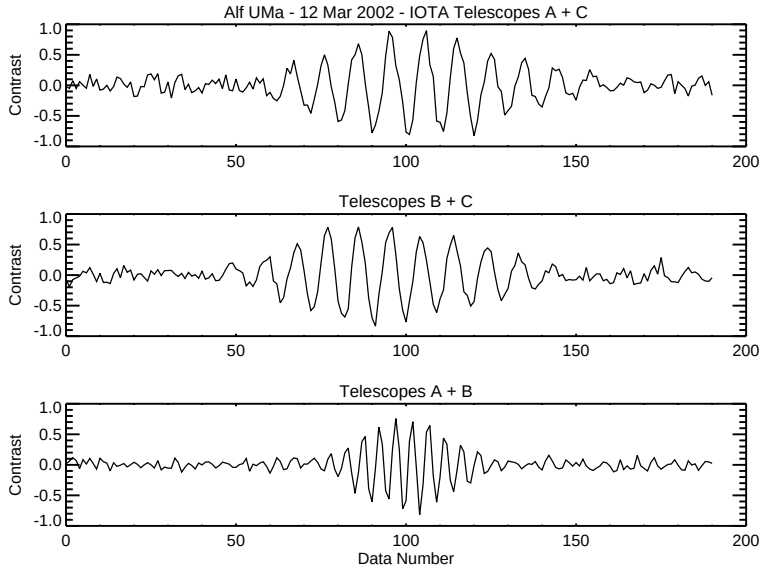

Fig. 6.— An example of H-band scans obtained using the CPLD interferogram readout circuit. These data were obtained using the IONIC-3T combiner (Berger et al. 2002). Complementary fringes for each telescope pair have been subtracted to enhance the SNR.

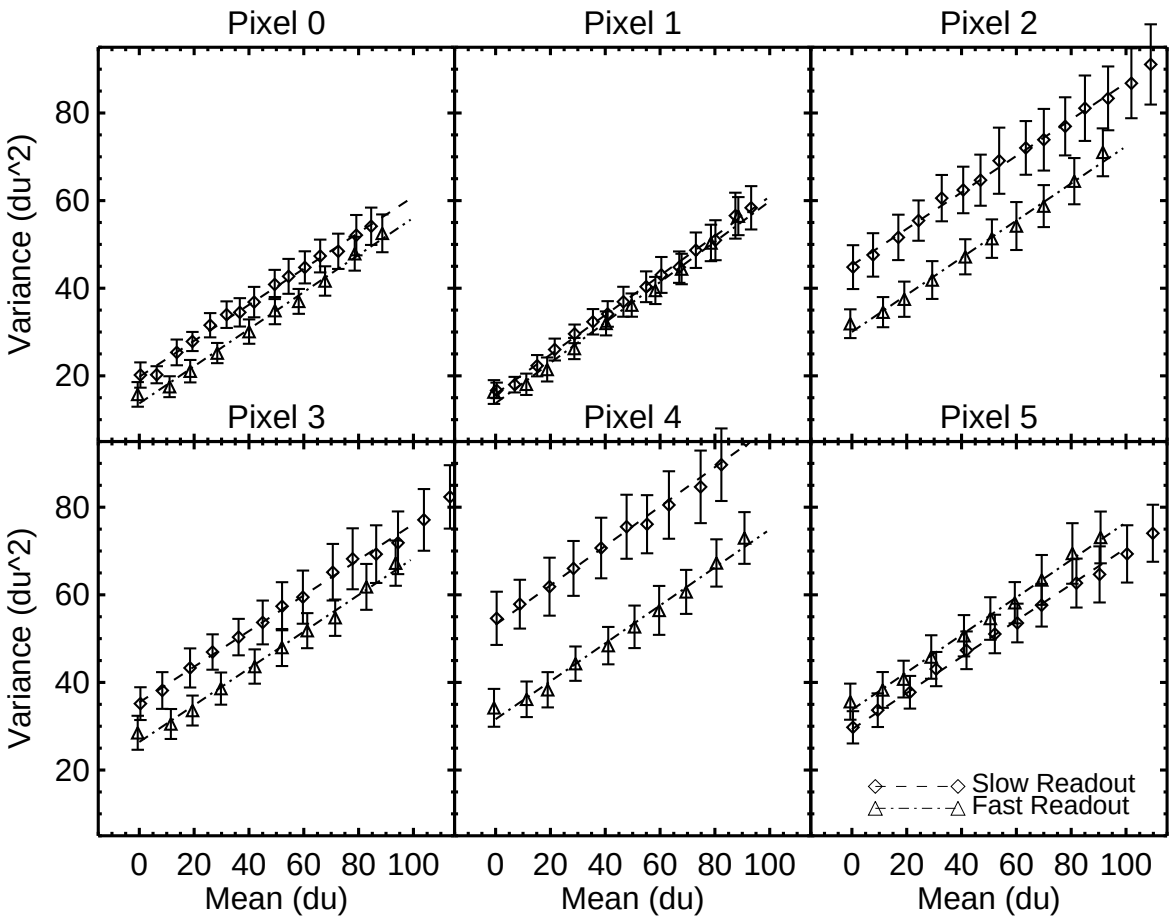

Fig. 7.— Variance vs. mean plot to measure system parameters. Data are plotted for six pixels sampled in interferogram mode. The two data sets in each plot were obtained for: (a) a slow readout mode (390 KHz PICNIC clock speed and 15 μs pixel sampling delay) and (b) fast readout (1 MHz clock speed and 4 μs pixel sampling delay). In each case, the slope provides the camera gain (elec/adu) and the y-axis intersect provides the read noise; the resulting gain and read noise values are listed in Table 4.

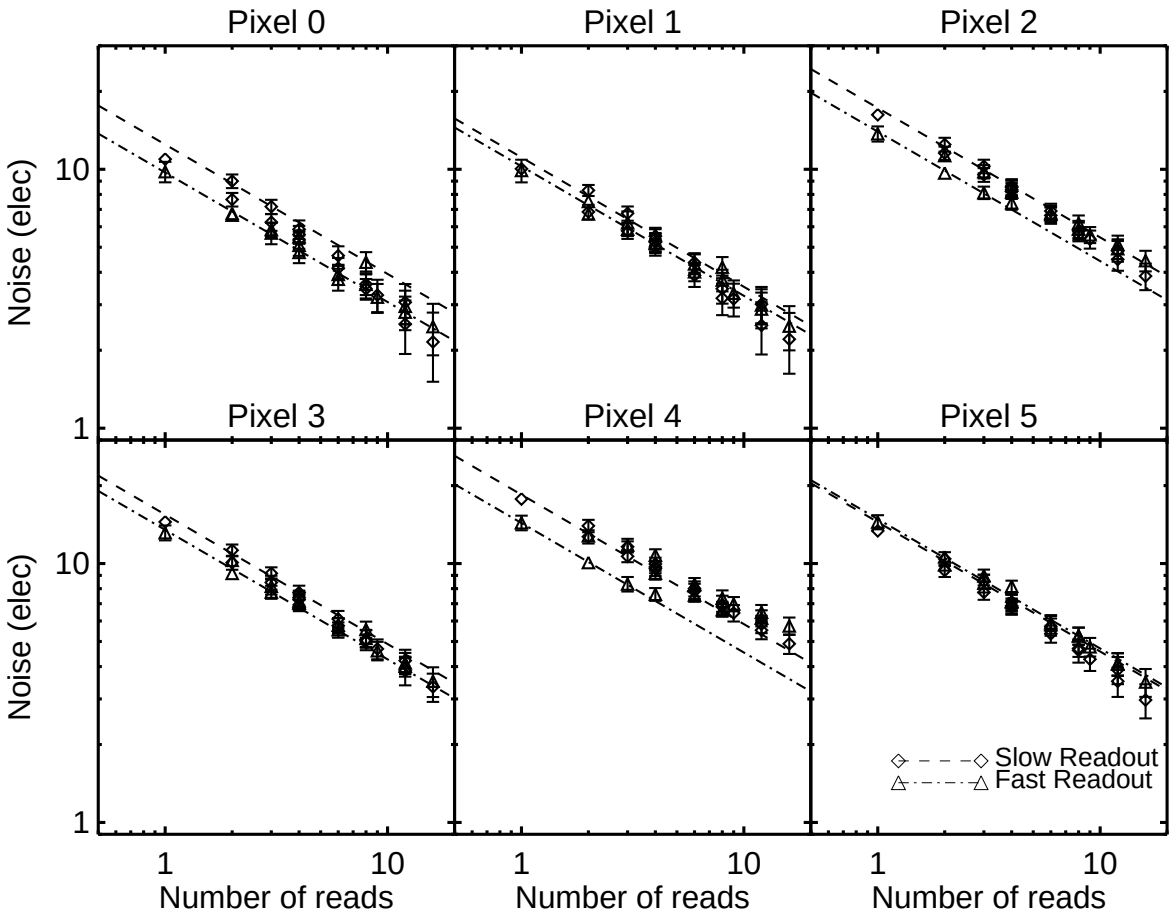

Fig. 8.— PICNIC camera measurements of scan rms versus number of reads, under zero illumination, for six pixels read in interferogram mode. As can be seen, noise reduction follows closely the ideal relation ($noise \approxeq 1/\sqrt{reads}$) plotted in dashed-lines.

Instruction	Hex Value	Action
fsync	02	FSYNC pulse generated
lsync	03	LSYNC pulse generated
line	00	LINE clock transition n-times
pixel	01	PIXEL clock transition n-times
jump	04	Jump to program location

Table 1: CPLD micro-coded instructions used to generate scanning sequences in interferogram readout mode.

Addr.	Hex Value	Mnemonic
0:	203;	– fsync + line 3
1:	302;	– lsync + pixel 2
2:	103;	– pixel 3
3:	004;	– line 4
4:	302;	– lsync + pixel 2
5:	103;	– pixel 3
6:	400;	– jump 00

Table 2: Arbitrary clocking sequence written using the instruction described in Table 1. The first instruction (address “0”) resets the line register and clocks three lines down. The second instruction resets the pixel register and clocks two pixels to the right. The third instruction clocks other three pixels to the right. Then the detector is clocked down of other four lines and at address “4” the pixel register is reset and the pixel clocked two positions to the right. Then the pixel is clocked other three positions to the right and at address “6” the program jumps back at instruction “0’ to restart the whole cycle again.

Loops \ Reads	1	2	3	4
1	340	510	670	830
2	660	990	1320	1640
3	980	1470	1960	2450
4	1300	1950	2610	3270

Table 3: The integration time (μs) as a function of the number of loops and reads derived from Equation (1). These values agree with the experimental data at about the 3% level.

Pixel	t_{int} (μs)	σ_{read} (elec)	g (elec/adu)
0	310	10.81 ± 0.26	2.43 ± 0.05
1	310	8.82 ± 0.17	2.22 ± 0.03
2	310	16.15 ± 0.27	2.40 ± 0.04
3	310	14.62 ± 0.25	2.46 ± 0.04
4	310	16.21 ± 310	2.22 ± 0.04
5	310	13.09 ± 0.24	2.42 ± 0.04

Pixel	t_{int} (μs)	σ_{read} (elec)	g (elec/adu)
0	130	8.74 ± 0.36	2.36 ± 0.08
1	130	8.04 ± 0.37	2.17 ± 0.07
2	130	12.93 ± 0.45	2.36 ± 0.08
3	130	12.25 ± 0.43	2.38 ± 0.08
4	130	12.98 ± 0.54	2.31 ± 0.09
5	130	13.58 ± 0.40	2.34 ± 0.07

Table 4: Results of read noise σ_{read} and camera gain g measurements. The noise is given per double read, given the differencing of consecutive samples intrinsic to our sampling method. Averaging over both integration times, the average read noise is $\sigma_{read} = 12.4 \pm 0.8$ elec and the average gain is $g = 2.34 \pm 0.03$ elec/adu.